Optimization of High Speed Carbon Nanotube Simple Inverter based Level Shifter

Bhavana P Shrivastava
Maulana Azad National Institute of technology,ECE Department,Bhopal
sonibhavana1@gmail.com

Abstract: In this paper a Level shifter is design to mitigate power consumption in System-on-Chips (SoCs) by applying proper technique to reduces additional power consumption and propagation delay in the circuit. Carbon Nano-tube material have one of the best property that provides variable Threshold Voltage (V_{TH}) to change V_{TH} of both PMOS Pull Up Network (PUN) and NMOS Pull Down Network (PDN) of transistor. In this research paper, the power and speed of CNT-FET based level shifters at 32-nm technology is calculated. It can increase the overall performance of the circuit by optimising the parameter like chirality, diameter, number of nanotubes and substrate (back gate) bias for both feedback-based and multi-V_{TH} based level shifters. Proposed circuit provides amplification of signal by applying input 0.2V and shifts the level to 0.9V without degradation of logic level of the signal. By applying back gate bias, minimum PDP is obtained by SI-LS i.e. 0.0028aJ which is thelowest PDP among all CMOS and FinFET technology.

Keywords: Leakage Power, CNTFET, Chirality, SI-LS, PDP, EDP.

Introduction

Nowadays as device sizes shrinks, the number of transistor get doubled every year according to Moore's law, so power consumption increases due to millions of transistor fabrication on a single IC chip. So, proper technique must be incorporated for minimization of power in circuits. Total power consumption in CMOS circuit is due three main component i.e., dynamic power, short circuit power and static or leakage power consumption. The dynamic power consumption is directly proportional to power supply. Scaling the power supply in circuit is most dominating method for reducing the dynamic and short circuit power consumption, but propagation delay of circuit increases [1] due to lower transistor current and reduction in clock frequency [2]. Two most popular types of scaling in VLSI technology are constant field scaling and constant voltage scaling. By scaling the supply voltage of the critical path the speed of circuits reduces. To overcome this problem multi-VDD system is used, in this case critical path is provided with standard power supply (VDDH) and supply voltage (VDDL) of non-critical path is scale down [3,4]. This makes different voltage level [5] and in order to communicate among each other, a voltage level converter is required for interfacing the circuit, and these circuit are called level shifter (LS) in low power circuit design.

Carbon nanotube based FET i.e. CNTFET is best material to replace the silicon based MOSFET circuit due to its quasi-ballistic transportation ability, negligible temperature dependency, high carrier mobility, high current density, easy integration with high-k dielectric material with easy fabrication feasibility [15, 16]. CNTFET has lower intrinsic gate-delay, energy consumption, OFF current and variableV_{TH} threshold voltage is one of the best property that can be used in multi threshold voltage or different threshold voltage for different transistor [17, 18] for reduction of power consumption.

In this research paper, basic circuitry are used for minimizing Power Delay Product (PDP) is Simple Inverter based level shifter (SI-LS) that are used in multi-V_{TH} technique [11].The circuit is designed with CNTFET to enhance performance of the CNT over silicon on ordinary MOSFET i.e. reduction in delay and power.

Carbon has two allotropes graphene and diamond, CNT has a perfect crystalline structure that contains strong covalent C-C bond. CNT has made-up with benzene structure of graphene which is single free electron (e^-)and arrangement of multiple benzene makes three configuration of CNT which define different property for different configuration i.e. (a) Zig-Zag have a sheet of graphene with horizontal benzene structure by joining two edges of benzene (b) Armchair have sheet of graphene with vertical benzene making structure like chair. (c) Chiral have sheet of graphene with slightly tilted benzene structure. The main objective of this paper is to calculate leakage power consumption with various leakage reduction techniques over CMOS and FinFET devices. CNTFET can be applied on high performance, low power applications where leakage is major concern such as microprocessor, memory units and other portable devices. The rest of this paper is organized as follows. Study of properties of CNTFET i.e. diameter, threshold voltage control, chirality vector, SI-LS circuit in section II. Study of various optimization technique of CNT-FET based Level Shiftersin section III. In Section III working of proposed circuit is disused. Section IV is of results and discussion; here leakage power is calculated by using FinFET (HP and LSTP library) technology. Finally, conclusion is offered in Section V.

CNTFET

Carbon Nanotube (CNT) is made-up of rolling a sheet of graphene. On the basis of number of concentric layers of CNT, it is called Single-Walled or Multi-Walled CNT and on the basis of vector direction a_1 and a_2 of rolling a sheet (also called chirality), it can act as metallic or semiconducting. The chirality index (m, n) is used to identify the direction of rollingof graphene sheet as shown in Fig.1. The carbon nanotube is metallic if m=n or the difference (m-n) = 3k where k is an integer, otherwise it act as semiconducting material [18]. Conductive or metallic is used as connection wire on-chip and semiconducting CNTs are used as channel of transistor or SWCNT and MWCNT channel. The diameter of CNT is given by equation (1)[15]

$$D_{CNT} = a\sqrt{\frac{m^2+n^2+mn}{\pi}} \quad (1)$$

Where *m* and *n* are chirality index of CNT and *a* is the lattice constant (2.49 ´). Fig.1 2D Graphene structure on the basis of chiral vector. Top view of CNTFET are shown in Fig. 2.

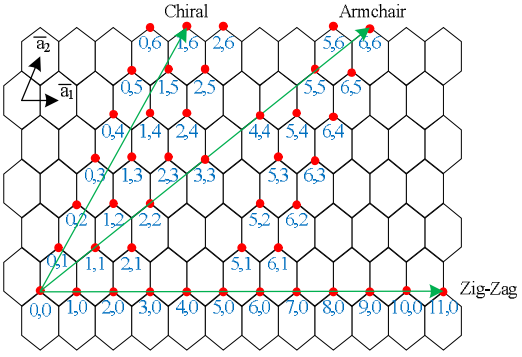

Fig.1 2D Graphene structure on the basis of chiral vector.

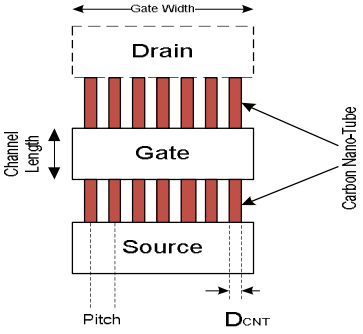

Fig.2 Top view of CNTFET

Andwidth of the CNTFET gate (W_{gate}) is calculated from equation (2)

$$W_{gate} \approx \text{Max}(W_{min}, N \times Pitch) \quad (2)$$

Where *Pitch* is the distance between Centres of two neighbouring SWCNT under same gate, W_{min} is minimum gate width and *N* is the number of Nanotube.

The layout of CNTFET is approximately similar to traditional MOSFET exceptchannel whichis formed between source and drain region is completely replaced by Carbon Nanotube. The source and drain region of the CNT are heavily doped which are used to interconnect with intrinsic CNT using heavily doped CNT interconnects. The intrinsic CNT forms the channel by enclosing with planer metal gate by high-*k* dielectric like zirconium oxide (ZrO_2) and hafnium oxide (HfO_2). Then substrate are fully covered by insulating thick SiO_2 layer. A single CNTFET channel is formed by multiple nanotube which are paralleled and aligned in accordance with the width of gate. The distance between centres of adjacent nanotube is called the pitch. In simulation work, source and drain are heavily doped CNTs with 0.8% doping level, HfO_{2is}used as gate dielectric having thickness 3*nm* and bulk dielectric SiO_2having thickness 10μ*m* [17]. CNT has a property that its energy gap (E_g) is inversely proportional to its diameter which allows to alter its band-gap by varying the diameter of CNTs. The threshold voltage (V_{TH}) of the CNT-FET can be approximated as half of the CNT band-gap [8, 9] as

$$V_{TH} = \frac{E_g}{2q} = \frac{1}{2\sqrt{3}}\frac{aV_\pi}{qD_{CNT}} \quad (3)$$

Where $V_\pi = 3.033\,eV$ the carbon-carbon bond energy and q is the electronic charge and b values,the equations can be simplified into y substituting these constant

$$E_g = \frac{0.872}{D_{CNT}} \text{And} V_{TH} = \frac{0.436}{D_{C\ T}} \quad (4)$$

Where,D_{CNT} is in *nm*. Thus, by changing the diameter of CNT, the threshold voltage and energy gap of CNTs arechanged and I_{ON}-current of device can be controlled. By increasing the diameter of CNTs, the threshold voltage decreases and I_{ON}-current increases because the sub-band of the channel becomes closer and more number of sub-band can shift towards fermi energy level [21]. This diameter-dependency of threshold voltage of CNT-FET makes the multi-VTH implementation of CNT-FET based circuits to be easier. Once therequired chirality(ordiameter)is fixed, ways toincrease current is that thenumber ofnanotubes should be increased andthepitchofthenanotubes is fixed atanoptimumvalue. Due to smaller pitch there is higher packingdensityofthenanotubes and at the same timetheON-current is reduced because of thescreeningof the gate field lines bythe neighbouring nanotubes when they come closer [9].

Another unique feathers of CNTFET is that the mobility of both p-channel and n-channel is approximately same and due to this I_{ON} and I_{OFF} currents are same for identical dimensions [23].Thisisbecauseof symmetry of electron-hole inCNT band

structure forsmallrangeofenergies which is closetotheFermi energy where mostofthephysicsofdeviceoperationliearound [24]. Since both type of CNTFET can draw same current, so p-channel CNTFET does not requireany sizing with respect to n-channel CNTFET for producing same current. Thus, various physical phenomena like quantum confinement, phonon scattering, band-to-band tunneling, charge screening and non-ideal ties like channel elastic scattering, parasitic resistances and capacitances are account into CNTs.

Level shifters using CNT-FET

Simple Inverter based Level Shifters (SI-LS)

The schematic diagram of SI-LS is shown in Fig.3. This circuit constitute multi-V_{TH} technique that has two stage of cascaded inverter i.e. inverter-I followed inverter-II. In inverter-I the PMOS X1 has shown by narrow tube indicating smaller diameter for higher threshold voltage. The working of SI-LS is that when low swing input voltage (0 to V_{DDL}) is given to inverter-I then it gives high swing inverted output voltage at node A (V_{DDH} to 0) which acts as input for inverter-II and whose output is proper up-converted form of input voltage i.e. 0 to V_{DDH}. Here importantthing is that threshold voltage PMOS X1 should be higher than the difference of (V_{DDH}-V_{DDL}) to reduce static leakage current and inverter-II need to be proper sized to reduce loading effect on inverter-I. The important in SI-LS circuit is that the sizing of all CNTFET should be proper to reduce static current.

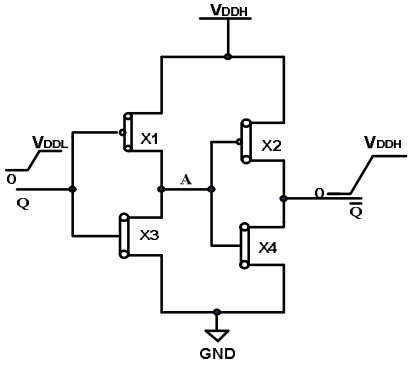

Fig.3 Simple inverter based level shifter

Optimization of CNT-FET based LEVEL SHIFTERS

SI-LS are optimized individually by two method [28] i.e. (a) By adjusting the number of nanotube (N) of PUN and PDN (b) By adjusting the back gate (substrate) bias of CNTFET. Optimization is made for input voltage V_{DDL} of 0.2V which is shifted up to 0.9V. Some of the chirality that is used in circuit, their diameter and threshold voltages are listed in Table.I and are calculated using equation (1) and (3).

Table. 1. List of chirality used in the circuits, their diameter and threshold voltage

Chirality	Diameter	V_{TH} (V)	$E_g(eV)$
(4,0)	0.313	1.392	0.626
(7,0)	0.548	0.795	1.096
(10,0)	0.783	0.556	1.566
(13,0)	1.018	0.428	2.036
(16,0)	1.251	0.348	2.502
(19,0)	1.486	0.293	2.972
(22,0)	1.720	0.253	3.440
(25,0)	1.955	0.223	3.910

Optimization of SI-LS

In optimization of SI-LS based circuit first chirality index (7, 0) of PMOS transistor (X1) in inverter-I is made to avoid static leakage current. This is due to V_{DDL}=0.2V and V_{DDH}=0.9V, to reduce leakage static power dissipation, the threshold voltage of X1 transistor should be larger than the difference between two i.e. 0.7V andV_{TH}=0.795V with chirality index (7, 0). When

the chirality index of NMOS (Inverter-I) i.e. X3 is fix at (25, 0) and number of Nanotube is fixed N=30and Inverter-II of the transistor X2 and X4 with chirality index (13, 0) and number of Nanotube N=5 is fix and by varying the number of tube from N=1 to N=15 of PMOS (Inverter-I) i.e. X1. Propagation delay, average power consumption and PDP are shown in Table-VI. When number of nanotube of X1 transistor increases driving current increase and due to this delay and power dissipation will more in SI-LS based circuit. When transistor X1 have N=1 then minimum PDP =6.087 aJ is obtained.

When PMOS (Inverter-I) X1 transistor is fix with chirality index (7, 0) and N=5 PMOS and Inverter-II of both transistor i.e. X2 and X4 are fix with chirality index (13, 0), N=5 by varying the number of Nanotube (N=5 to N=40) of X3 transistor with chirality (25, 0) and propagation delay, average power consumption and PDP are shown in Table-VII. Similar trade-off between delay and power dissipation is observed in Table-VI and Table-VII. The minimum PDP 0.055 aJ is observed with N=5 for X3 transistor i.e. NMOS of inverter-I.

The analysis of loading effect of inverter-II on inverter-I, by varying of Nanotube of both X2 and X4 transistor i.e. PMOS and NMOS of inverter-II simultaneously and which shown in Table-VII. It is observed that the delay and power consumption reduces if the number of Nanotubes are less. Hence by choosing N=40 of inverter-II give lowest PDP of 0.0028 aJ. Another analysis is when back gate bias is applied to any inverter Ior II the PDP obtain value is 0.73 aJ which is minimum optimized value for SI-LS circuit.

Results and Discussion

All the simulation results are obtained by using BISM4, HSPICE model at 32nm by using Predictive Technology Model (PTM), which requires a spice code (transistor-level net-list) of the desired circuit for calculation of the parameters. In SI-LS circuit if tube of PMOS of inverter-I is increases then power consumption rapidly increases and delay also increase and overall PDP also increases which is shown in Table-II. If the number of tube of NMOS increase in inverter-I, then power, delay and overall PDP increases as shown in Table-III. In SI-LS circuit if number of tube of inverter-II is increases then power consumption will constant at higher value of N and delay reduces and overall PDP will decrease and minimum PDP is obtained at N=40 of inverter-II and inverter-I have N=10 and minimum PDP is 0.0028 aJ that's are shown in table-IV.

In DCVS-LS circuit, when back gate bias voltage is applied to substrate of both PMOS and NMOS transistor, it acts like secondary gate of CNTFET. If the positive back gate bias voltage increases from 0 to 0.9V keeping number of tube of PUN fixed at N=4 and number of tube of PDN are fixed at N=40 then power and delay get increased by that the overall PDP increases. If the negative back gate bias voltage increases from 0 to 0.9V then both power and delay get decreased and due to this the overall PDP decreases which as shown in Table-IV. Similarly, if PDN is fixed at N=25 then power and delay increases due to this the overall PDP increases with positive back gate bias voltage. Power and delay decrease and overall PDP decrease with negative back gate bias voltage which are shown in Table-V.

Table 2. SI-LS by varying N of PMOS of inverter-I V_{DDH}=0.9V, V_{DDL}=0.2V PMOS (7, 0) Pitch=20nm, NMOS (25, 0) N=30, Pitch=20nm and inverter-II (13,0), N=5

N=NO. of tube in PMOS Inverter-I	Power (nW)	Delay (ps)	PDP (aJ)	EDP (E-30 J)
1	136.24	90.48	12.326	1115.347
2	141.85	90.97	12.904	1173.885
3	141.85	90.98	12.905	1174.144
4	149.57	94.56	14.143	1337.394
5	161.72	98.58	15.942	1571.598
6	169.81	100.1	16.997	1701.498
7	179.74	102.3	18.387	1881.031
8	188.82	104.6	19.750	2065.91
9	201.36	106.7	21.485	2292.461
10	209.24	109	22.807	2485.98
11	221.27	111.2	24.605	2736.101
12	231.47	108.9	25.207	2745.051
13	245.22	111.3	27.292	3037.709
14	263.78	113.1	29.833	3374.171
15	284.99	115.2	32.830	3782.114

Table 3. SI-LS by varying N of NMOS of inverter-I,V_{DDH}=0.9V, V_{DDL}=0.2V PMOS (7, 0) Pitch=20nmN=5,NMOS (25, 0) Pitch=20nm and inverter-II (13, 0), N=5

N=NO. of tube in NMOS Inverter-I	Power(nW)	Delay (ps)	PDP (aJ)	EDP (E-30 J)
5	20.02	3.494	0.069	0.2444
10	32.32	11.34	0.366	4.1573
15	58.69	39.449	2.315	91.348
20	94.56	69.562	6.577	457.56
25	127.3	87.924	11.19	984.34
30	161.7	98.562	15.93	1571.0
35	194.2	107.41	20.86	2241.1
40	226.7	116.53	26.41	3078.5

Table 4**.** SI-LS by varying N of inverter-II,V_{DDH}=0.9V, V_{DDL}=0.2V PMOS (7, 0) Pitch=20nm, NMOS (25, 0) Pitch=20nm N=10

N=NO. of tube in Inverter-II	Power (nW)	Delay (ps)	PDP(aJ)	EDP (E-30 J)
5	29.19	8.97	0.2618	0.1547
10	21.29	2.67	0.0568	2.3517
15	18.55	1.04	0.0192	10.735
20	18.38	0.501	0.0092	43.595
25	18.44	0.413	0.0076	165.70
30	18.37	0.296	0.0054	447.39
35	18.43	0.171	0.0031	1124.69
40	18.45	0.153	0.0028	2122.55

Comparison with FinFET based Level Shifters

FinFET is a non-planar 3D structure that contains thin vertical channel that resembles Fish's Fin surrounded by gate. Alongthese sides forms Drain and Source unlike MOSFET the conducting channel gate is wrapped around the Fin allowing very less leakage of current through the body during OFF state and provides better control over the channel. Fabrication of double gate by using a process of lithography, gate is easily wrapped over the silicon fin. Front gate and back gate have different doping profile, so both gate operate independently according to the requirement. One of the main challenges in making FinFET over bulk-CMOS is that it has large number of capacitance associated, like fringing and overlapping capacitance due to which the resistance of FinFET increases. Table-IX shows all the parameter taken into consideration during the simulation of FinFET technology.

The performance comparison of CNTFET with silicon based device i.e. FinFET based level shifter circuit with FinFET having V_{DDL}=0.5V and V_{DDH}=0.9V is observed by using BSIM-common Multi-Gate (BSIM-CMG) technology. FET model [27] is used for simulation and comparison with CNTFET based level shifter.

Table 5. Device Parameters of 32nm Double gate NMOS and PMOS MSFET

Parameter	32nm DGN MOSFET	32nm DGP MOSFET
Channel length from Source to drain(L)	32nm	32nm
Channel length(L_{eff}) where gate is wrapping over thin silicon Fin	25.6nm	25.6nm
Thickness of the Fin (t_{si})	8.6nm	8.6nm
One face Height of Fin (H_{fin})	40nm	80nm
Silicon oxide thickess (t_{ox})	1.4nm	1.4nm
Threshold voltage V_{TH} (V)	0.29	-0.25

Table 6. Comparison of level shifter SI-LS in delay, power and PDP

Circuit		Power (nW)	Delay (ps)	PDP (aJ)
FinFET	SI-LS	22.83	19.28	0.440
CNTFET	SI-LS	18.45	0.153	0.0028

Above Table shows that CNTFET has superior electrical characteristic to replace both CMOS and FinFET technology in terms of power and speed of circuit.

Conclusion

As the demand of low power consumption, battery operated device and high speed CNTFET comes into existence for minimization of technology.. As the number of tubes increase of SI-LS in inverter-II the power consumption reduces drastically up to 98.93% and propagation delay is reduced by 98.29%. The result of FinFET and CNTFET is also compare in terms of PDP, we observe that CNTFET has 99.36% SI-LS. This result shown in Table-6.

References

[1] J. Rabaey, A.Chandrakasan, B. Nikolic, Digital integrated circuits: a design perspective, 2nd edition, Prentice Hall, New Jersey, 2003.

[2] S. Wooters, B. Calhoun, T. Blalock, An energy-efficient subthreshold level converter in 130-nm CMOS, IEEE Trans. Circuits Syst. II: Express Br. 57 (4) (2010) 290–294.

[3] Wang, A. Chandrakasan, S. Kosonocky, Optimal supply and threshold scaling for subthreshold CMOS circuits, in: Proceedings of the IEEE Computer Society Annual Symposium on VLSI, 2002, pp. 5–9.

[4] V. Kursun, E.G. Friedman, Multi-voltage CMOS Circuit Design, John Wiley & Sons, New York, 2006.

[5] D.E. Lackey, et al., Managing power and performance for system-on-chip designs using voltage islands, in: Proceedings of the IEEE/ACM International Conference on Computer Aided Design, 2002, pp. 195–202.

[6] K. Koo, J. Seo, M. Ko, J. Kim, A new level-up shifter for high speed and wide range interface in ultra-deep sub-micron, in: Proceedings of the IEEE Inter-national Symposium on Circuits and Systems, 2005, pp. 1063–1065.

[7] T.H. Chen, J. Chen, L. Clark, Subthreshold to above threshold level shifter design, J. Low Power Electron. 2 (2) (2006) 251–258.

[8] Y.Sun, V. Kursun, N-type carbon-nanotube MOSFET device profile optimization for very large scale integration, Trans. Electr. Electron. Mater. 12 (2) (2011) 43–50.

[9] Y. Sun, H. Jiao, V. Kursun, A novel robust and low-leakage SRAM cell with nine carbon nanotube transistors, IEEE Trans. Very Larg. Scale Integr. (VLSI) Syst. 99 (2014)

[10] S.R. Hosseini, M. Saberi, R. Lotfi, A low-power subthreshold to above-threshold voltage level shifter, IEEE Trans. Circuits Syst. II: Express Br. 61 (10) (2014) 753–757.

[11] S. Tawfik, V. Kursun, Low power and high speed multi threshold voltage interface circuits, IEEE Trans. Very Larg. Scale Integr. (VLSI) Syst. 17 (5) (2009) 638–645. S.C. Luo, C.J. Huang, Y.H. Chu, A wide-range level shifter using a modified Wilson current mirror hybrid buffer, IEEE Trans. Circuits Syst. I: Regul. Pap. 61 (6) (2014) 1656–1665.

[12] J. Zhou, C. Wang, X. Liu, X. Zhang, J. Minkyu, An ultra-low voltage level shifter using revised Wilson current mirror for fast and energy-efficient wide-range voltage conversion from sub-threshold to i/o voltage, IEEE Trans. Circuits Syst. I: Regul. Pap. 62 (3) (2015) 697–706.

[13] M. Lanuzza, P. Corsonello, S. Perri, Fast and wide range voltage conversion in multi-supply voltage designs, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 23 (2) (2015) 388–391.

[14] J. Deng, H.S.P. Wong, A compact spice model for carbon-nanotube field-effect transistors including non-idealities and its application – part 1: model of the intrinsic channel region, IEEE Trans. Electron Devices 54 (12) (2007) 3186–3194.

[15] A.D. Franklin, M. Luisier, S.-J. Han, G. Tulevski, C.M. Breslin, L. Gignac, et al., Sub-10 nm carbon nanotube transistor, Nano Lett. 12 (2) (2012) 758–762.

[16] J. Deng, H.S.P. Wong, A compact spice model for carbon-nanotube field-effect transistors including non-idealities and its application – part 2: full device model and circuit performance benchmarking, IEEE Trans. Electron Devices 54 (12) (2007) 3195–3205.

[17] Y. Sun, V. Kursun, Carbon nanotubes blowing new life into np dynamic CMOS circuits, IEEE Trans. Circuits Syst. I: Regul. Pap. 61 (2) (2014) 420–428.

[18] S. Lin, Y.B. Kim, F. Lombardi, Design of a ternary memory cell using CNTFET, IEEE Trans. Nanotechnology. 11 (5) (2012) 1019–1025.

[19] S. Datta, Quantum Transport: Atom to Transistor, Cambridge University Press, New York, 2005.